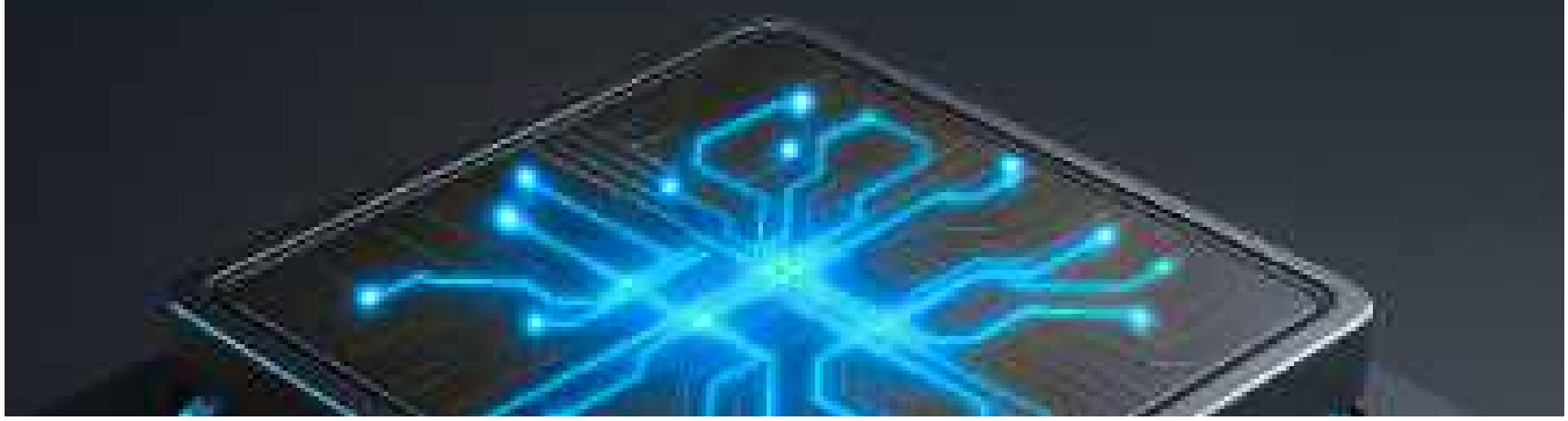
PHOTONIC AI CHIP PLATFORM

Design and Functionalitaty Validation of an On-Chip Matrix Multiplication Engine for Optical Inference Acceleration



WHITEPAPER LAUNCH

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QUANTLASE
RESEARCH AND DEVELOPMENT CENTER

The UAE's first fully validated, industry-grade, purpose designed photonic matrix multiplication chip , aligned to European chip manufacturing standards, and embedded in a real-world manufacture–test–package pipeline. A foundational step towards a manufacturable, scalable and energy efficient photonic computation for AI workloads.

1. This Whitepaper at a Glance

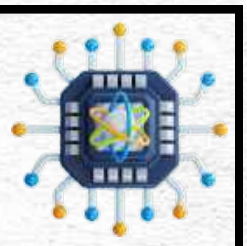
About this Whitepaper

- ☑ Introduces UAE's first industrial photonic chip blueprint, to the best of knowledge
- ☑ A concrete first step towards hardware AI
- ☑ Middle East's first photonic chip tech whitepaper prepared to global industry standard, to the best of knowledge

Strategic Significance of This Work

- ☑ Foundational step towards AI hardware backbone
- ☑ It matters now, given the focus on AI innovation
- ☑ A foundation of industrial-grade, home-grown photonic chip innovation

What this whitepaper reports?



- ☑ An execution from thought to hardware - backed by metrics
- ☑ Validated matrix operations using first-time-right simulations
- ☑ Design committed to chip manufacture already - Export compliance confirmed

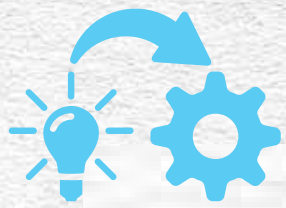
Next milestones

- ☑ Delivery schedule Jan'26 for industry grade photonic chips
- ☑ Full chip testing and characterization Mar'26
- ☑ Fully packaged and tested matrix multiplication chip modules, May'26

Why this work matters to the global chip industry?

- ☑ Bridges UAE origin chip architecture to European Manufacturing
- ☑ Offers hybrid model: Local design, global execution
- ☑ Enables chip rapid lifecycle innovation led from the UAE

4. From Ambition to Execution: A Novel Pathway to Sustainable Photonic Compute Infrastructure



1

The Ambition: A Photonic Computing Infrastructure for the Region

The long-term goal is clear: to enable sovereign photonic computing infrastructure, capable of handling advanced AI workloads through light-based data processing.

But such ambition must be built on a sustainable foundation and a strong synergy between software and hardware fronts

2

The Gap: Innovation Trapped in the Lab

Current research in optical computing, though technically impressive, is often not designed with manufacturing, export control, or real-world integration in mind.
Many architectures demand fabrication environments or use cases that cannot be replicated or shipped legally across borders.

Without a bridge to manufacturability, these innovations risk becoming immobile.

3

Our Approach: A Novel Path to Scalable, Compliant Execution

This work defines a first-of-its-kind balance: performance-driven design anchored in export-compliant, fabrication-aligned topology, manufactured via global pathways legally navigated and contractually secured.
The computing chip architecture in our whitepaper is not a theoretical novelty, but a purpose-built curated architecture that:

- Aligns with commercial foundry rules
- Avoids dual-use red flags
- Enables real chip packaging and testing

Each layer of the project, design, simulation, legal routing, and test-readiness is approached to de-risk the path from ambition to outcome

4

The Outcome: A Platform for Sustainable Hardware Sovereignty

Beyond a batch chip delivery and a hardware prototype, this work opens a foundational lane for future photonic chip programs:

- Design frameworks that align with global export norms
- Hardware architectures that can evolve without breaching compliance
- Ground-level experience that can guide future local infrastructure

This chip is the first executable layer of a long-term vision for scalable, sustainable, and sovereign photonic computing.

9. From Strategy to Execution: Where the Program Stands Today

The previous section laid out the layered logic that governed our design decisions, a structure that was not just theoretical but executed under live conditions with fixed deadlines, regulatory constraints, and with a fast development pace. That strategy has now materialized into clear, measurable outcomes. This orchestration is now visible in tangible outcomes. The snapshot below captures those outcomes across two dimensions:

On the left, a translation for broader stakeholders , what they can see as progress and what can be anticipated next.

On the right, a line-of-sight for chip professionals, with details on files, process design kits, and post-manufacture test plans.

This dual-view structure reflects how we have managed both visibility and technical accountability in parallel. We also aim to ensure the effort resonates across audiences without diluting the engineering integrity.

EXECUTION SNAPSHOT: WHAT IS DONE AND WHAT IS NEXT

Progress made on chip development:
For general audience

- ✅ Chip design confirmed
- ✅ Matrix multiplication operation confirmed
- ✅ Chip manufacturing underway
- ✅ UAE-EU chip export control regulation compliance confirmed
- ✅ Chip module assembly plan confirmed
- ⏭ Chips to be delivered in January next year
- ⏭ Extension to alternative material platform planned for viability and low cost production

Progress made on chip development:
For chip tech professionals

- ✅ GDSII files ready
- ✅ Foundry DRC passed
- ✅ Flexible MPW targeted on SiPho platform
- ✅ PDK choice confirmed
- ✅ ADK alignment confirmed
- ⏭ Chip tape-out in January'26
- ⏭ Parallel PDK on InP intercept planned for early 2026
- ⏭ TDK confirmation and test plan underway

However, orchestrating all moves form within UAE and moving physical hardware across borders in another continent is not just about technical understanding, it also requires regulatory alignment. As we finalize tape-out and prepare for packaging and international transit, compliance with global export laws becomes centric to program success. In high-stakes hardware programs like ours, success hinges not only on engineering milestones but on legal foresight. On the next page we list a breakdown of the export control strategy embedded within this program, so we ensure that our chips are delivered smoothly when they are built. Also this is exactly what differentiates a chip "you-make" from a chip "you-buy".

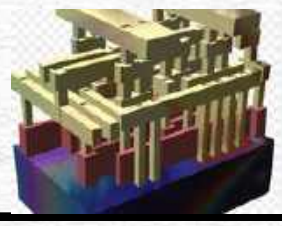
12. Chip Functionality Validation and Manufacturing Aligned Design Framework

Simulation Tools

- ☑ Synopsys Optisim - an industry grade award winning suite used for simulation
- ☑ Virtual prototyping for reduced time-to-market
- ☑ Interface with 3rd party tools i.e. MATLAB, able to generate layout

Design Methods

- ☑ Time domain analysis of interference phenomena
- ☑ Frequency domain analysis of MZI
- ☑ Chip layout and component routing compatible with chip manufacturing standards



Chip Design Parameters

- ☑ Chip waveguide propagation loss
- ☑ Grating coupler insertion loss
- ☑ 3 db coupler loss
- ☑ V_pi
- ☑ MZI phase tuning

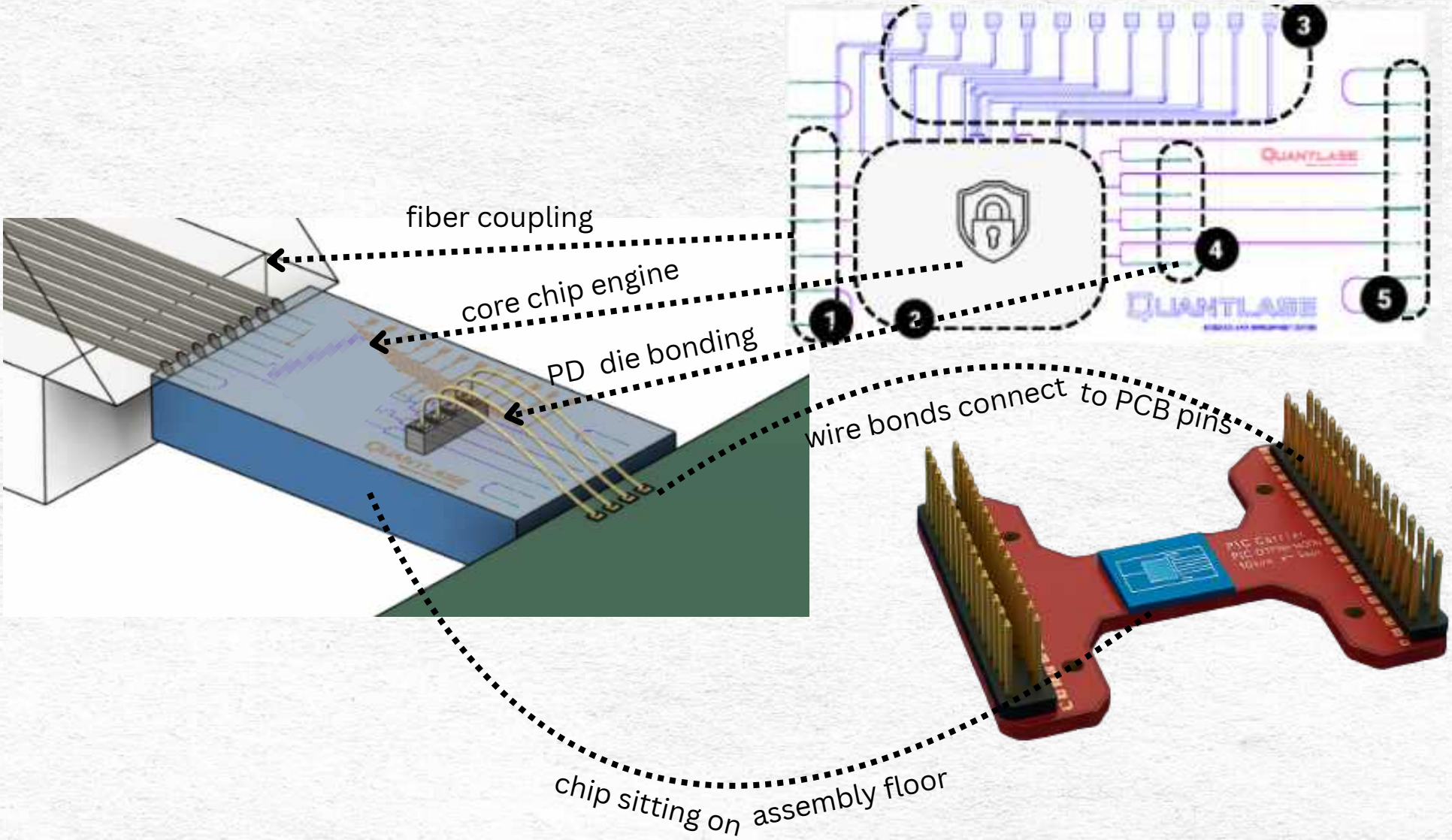
Design-Fabrication Alignment

- ☑ Device level (waveguides, modulators) fabrication stack aligned with EU chip foundry rules
- ☑ Chip layout geometry aligned with chip foundry PDK
- ☑ Chip design integration with manufacturing - test - package pipeline already established

This design and simulation framework is an industry aligned approach where actual chip operating conditions are embedded and the model is designed around validating the functionality of the computing chip. We only provide details necessary to prove chip functionality and a full in depth academic discourse is not the intent of this communication.

17. The Final Product Visual

Rendered via the assembly design kit of VLC Photonics - Hitachi Group, this visualization illustrates the final product form factor of our photonic matrix multiplication chip. The left image shows the fiber-array interface and Si/Ge photodetector bonding layout on the top of computing chip output waveguides. The right image presents the expected packaging format, where the chip is mounted onto a custom carrier with electrical pinouts for integration. Though the chip is currently undergoing fabrication, this visual reflects the validated mechanical and electrical design, offering a forward-facing glimpse of the deliverable hardware. It underscores our industrial alignment and accelerated execution model, where visualized outcomes guide design and manufacturing convergence from the outset.



Left: Assembly image of our chip design visualized as a finished chip (5 mm x 10 mm), the photodetectors are bonded onto the top of output waveguides. At a finalized stage of hardware packaging the wire-bonds connect onto the electrical pins show in the final housing on right. The chip is shown as the blue box sitting in the middle of the butterfly packaging.

While this is an early prototype milestone, it is one of significant consequence for the Middle East. It demonstrates that chip-scale photonic computing can be conceptualized, validated, and aligned for production using industry-grade design tools, partner infrastructure, and execution discipline all from within the region here.

At the same time, we acknowledge that some aspects such as full-system electrical test protocols, long-term reliability qualification, and mass-production scaling remain in development. These are well understood as post-prototype stages in photonic hardware programs globally, and our roadmap is calibrated to address them in parallel.

18. Architectural Context and Innovation Direction

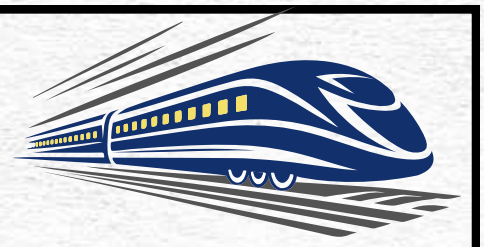
While the MZI mesh architecture used in this design has been documented in prior literature, and is not claimed here as a structural innovation, our implementation leverages it as a modular, fabrication-aligned platform to pursue a far more complex and differentiating challenge i.e. **the control layer**.

Specifically, our contribution lies in the system-level orchestration of the following:

- Weight assignment strategies across mesh stages that maintain functional linearity under practical constraints
- Phase tuning precision calibration, compatible with thermal tuning latency and physical tolerances
- The future integration of feedback-driven training loops, where output detection informs real-time phase adjustment, enabling dynamic inference, classification, or signal filtering tasks

In this framing, the mesh in itself is not a breakthrough structure, rather it is the hardware platform upon which we can execute programmable photonic control logic, mapped to real-world applications. This approach shifts focus from purely structural novelty to functional and operational innovation, which we believe unlocks the path to cutting edge in scalable photonic computing.

What do we mean by "control layer"?



Think of our chip like a high-speed railway system made of light. The tracks are fixed, and that is the mesh architecture. But how fast the trains go, where they switch tracks, and how they avoid crashing, that is the control layer.
In our chip, this control happens through tiny tunable elements that adjust the flow of light in real time.

- They decide which inputs go where.
- They assign weights, like adjusting how much importance each signal gets.
- And in future designs, these control mechanisms can even be extended to respond to feedback, enabling light-based systems that can adapt and learn from their environment.

So while many have shown similar tracks (the mesh), this work is about building the foundation of that real-time control logic. It is not just about routing light, it is about laying the groundwork for programmable and intelligent photonic computing.

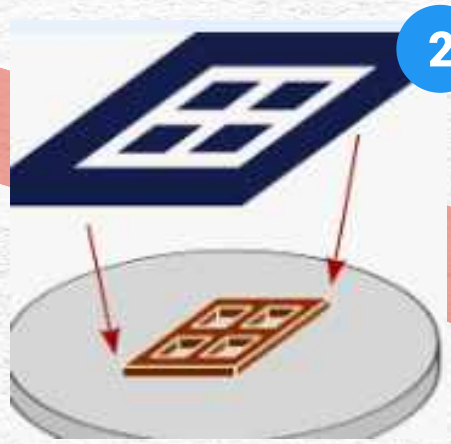
19. How is this chip manufactured...chip foundry based in EU

1

Silicon wafers - 8 inch

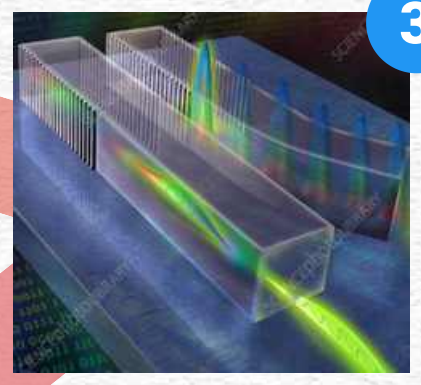
Pattern wafers - lithography

2



Create chip waveguides (etching)

3



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Deposit metal for device probing

Hundreds of chips fabricated over a wafer

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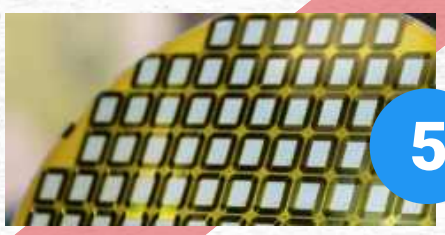

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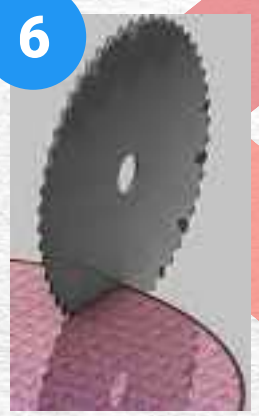
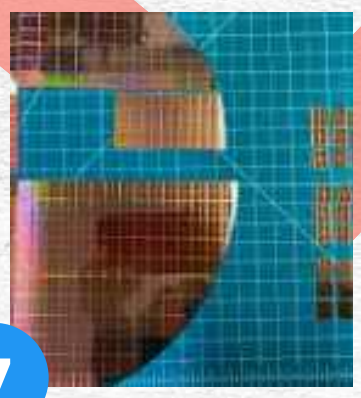


Wafer diced using mass-scribing

7



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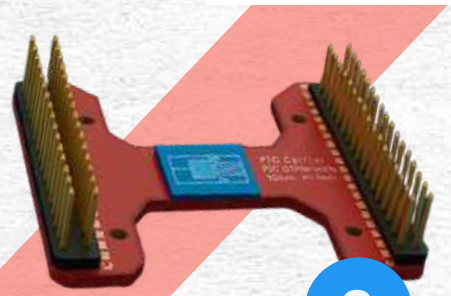

Chips wire bonded to module package

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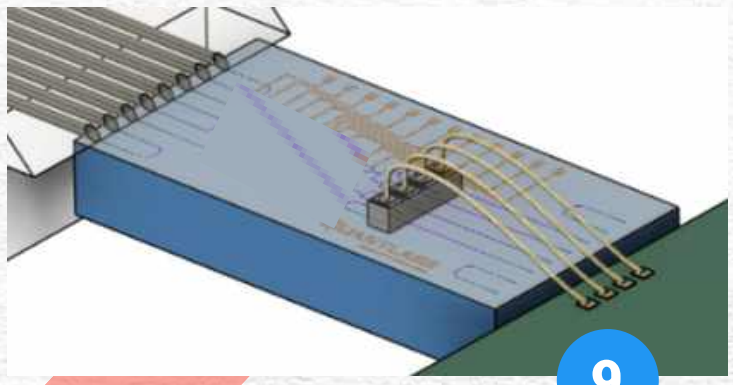
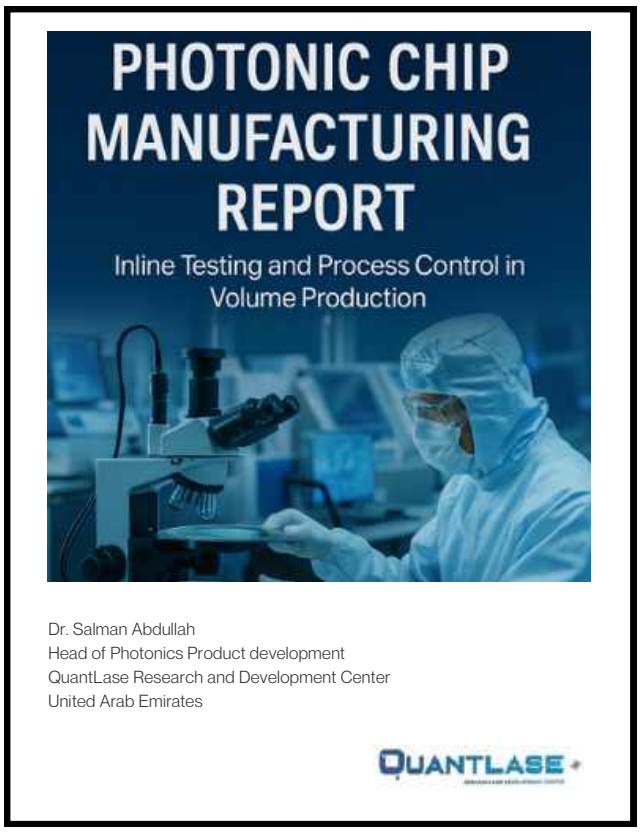


Individual chips diced

23. What execution story is next.....

This whitepaper inaugurates a strategically structured release series anchored in our development approach seeking to bring prototypes to market through an accelerated route. Rather than isolated reports, these publications are synchronized with real engineering milestones and guided by a reverse-mapped execution framework designed to compress development timelines. The next installments are centered on chip manufacturing and ecosystem integration respectively. The release plan is already approved and under execution, forming a cohesive narrative of how high-impact photonic hardware can be developed, validated, and positioned for production through a precision-engineered, fast-cycle roadmap. This series reflects an approach of architectural ownership from concept to industrial realization



Author's Note: This initiative would not have reached its current maturity without the strategic platform enabled at QRDC including resource alignment, executive backing, and insulation from delays typical in emerging tech programs. That clarity of direction made it possible to activate a rapid development pipeline now calibrated for industrial outcomes. The progress so far has been made possible by institutional alignment, not individual effort.

24. PROGRAM CREDITS

SHERAZ SIDDIQUI
EXECUTIVE DIRECTOR

PROGRAM STRATEGY

- Executive support for project, strategy direction and ROI expectations
- Provided clear ecosystem alignment vision of this project
- Approved rapid execution blueprint & ensured project insulated from admin delays
- Aligned executive org support to project phases

DR. PRAMOD KUMAR
DIRECTOR OF RESEARCH

TECHNICAL VISION AND PROJECT SUPPORT

- Provided full program vision for matrix multiplication chip scale project
- First regional vision for a broader roadmap on photonic intelligence enabled optical inference
- Technical milestone mapping on inference and training chip program
- Advised on matrix multiplication project phases and expected chip functionality
- Ensured prompt release of funds

DR. SALMAN ABDULLAH
HEAD OF PRODUCT DEVELOPMENT

TECHNICAL ARCHITECT& PROGRAM LEAD

- Develop chip design
- Design - Manufacture-Test-Package alignment of chip program to industry standards
- Prepared the matrix multiplication simulation framework and communication approach
- Assess export control landscape and routes to navigate EU-UAE channels
- Supply chain navigation and identification of rapid manufacturing cycles
- Author whitepaper